DOCKET NO.: 274525US2PCT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Sathwant DOSANJH, et al.

SERIAL NO.: NEW U.S. PCT APPLICATION

FILED: HEREWITH

INTERNATIONAL APPLICATION NO.: PCT/CA04/00025

INTERNATIONAL FILING DATE: January 8, 2004

FOR: REGENERATIVE DIVIDER FOR UP AND DOWN CONVERSION OF RADIO FREQUENCY (RF) SIGNALS

REQUEST FOR PRIORITY UNDER 35 U.S.C. 119 AND THE INTERNATIONAL CONVENTION

Commissioner for Patents
Alexandria, Virginia 22313

Sir:

In the matter of the above-identified application for patent, notice is hereby given that the applicant claims as priority:

COUNTRY	APPLICATION NO	DAY/MONTH/YEAR
Canada	2,415,917	08 January 2003

Certified copies of the corresponding Convention application(s) were submitted to the International Bureau in PCT Application No. PCT/CA04/00025. Receipt of the certified copy(s) by the International Bureau in a timely manner under PCT Rule 17.1(a) has been acknowledged as evidenced by the attached PCT/IB/304.

Respectfully submitted,
OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Marvin J. Spivak
Attorney of Record
Registration No. 24,913
Surinder Sachar
Registration No. 34,423

Customer Number
22850

(703) 413-3000
Fax No. (703) 413-2220
(OSMMN 08/03)

PCT/CA2004/000025
06 February 2004 06-02-04

Office de la propriété intellectuelle du Canada
Un organisme d'Industrie Canada

Canadian Intellectual Property Office
An Agency of Industry Canada

Bureau canadien des brevets

Certification

La présente atteste que les documents ci-joints, dont la liste figure ci-dessous, sont des copies authentiques des documents déposés au Bureau des brevets.

Canadian Patent Office

Certification

This is to certify that the documents attached hereto and identified below are true copies of the documents on file in the Patent Office.

Specification and Drawings, as originally filed, with Application for Patent Serial No: **2,415,917**, on January 8, 2003, by **SiRiFIC WIRELESS CORPORATION**, assignee of Tajinder Manku, Satiwant Dosanjh and William Kung, for "Regenerative Divider Used for Up-Conversion and Down Conversion".

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

REC'D 26 FEB 2004
WIPO PCT

Agent certificateur/Certifying Officer

February 6, 2004
Date

Canada

(CIPO 68)
04-09-02

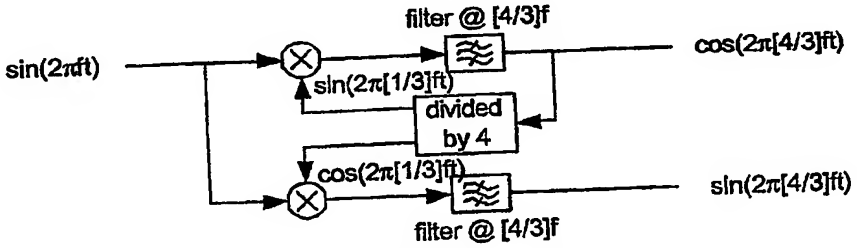
OPIC CIPO

Regenerative Divider Used for Up-Conversion and Down-Conversion

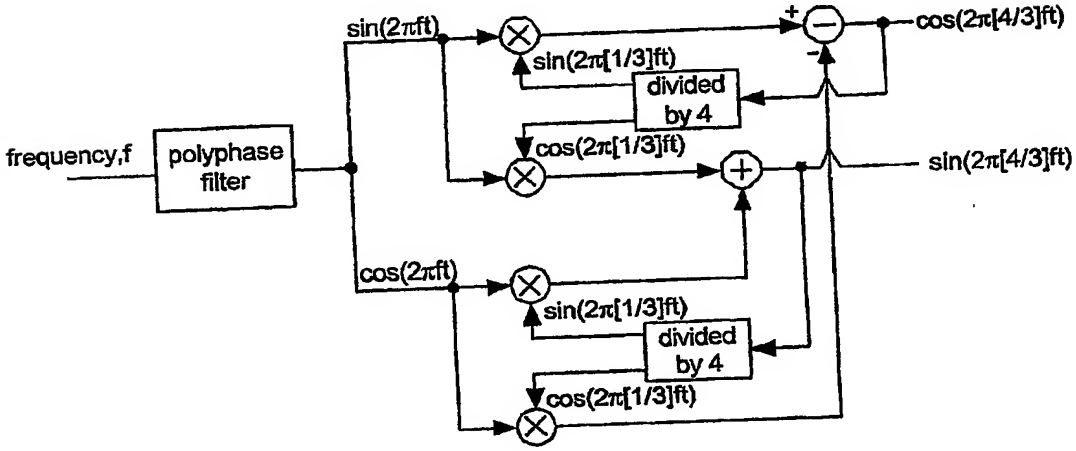
INTRODUCTION

This document describes a form of regenerative dividers that generate the quadrature components of the carrier frequency required in direct up or down conversion. The regenerative divider will be incorporated as part of Sirific's core technology (see PCT patent application serial no. PCT/CA00/00994, PCT/CA00/00995 and PCT/CA00/00996).

The two regenerative divider circuits are shown in Fig. 1. One is for narrow band cases and the other is for wide band cases. Both architectures use ¾ the carrier frequency as the local oscillators (LO) – denoted as frequency, *f*. The narrow band uses a divided by four element to generate the quadrature components at a frequency of 1/3 the LO frequency. The two branches (i.e. the top and bottom) should be as symmetric as possible. It may be necessary to attach a dummy divided "by 4 element" to the bottom arm to increase the amount of symmetry. The band-pass filter is centered at 4/3 the LO frequency (or the carrier frequency). This helps remove harmonics produced by the divided by 4 and the mixers (or multipliers). One of the harmonics that needs to be removed is the one at 1/3 the LO frequency. This harmonic can also be removed using a notch filter centered at 1/3 LO – see Fig. 2. In the wide band circuit the 1/3 LO frequency is removed using a quadrature subtraction technique. The poly-phase filter produces quadrature elements of the LO.

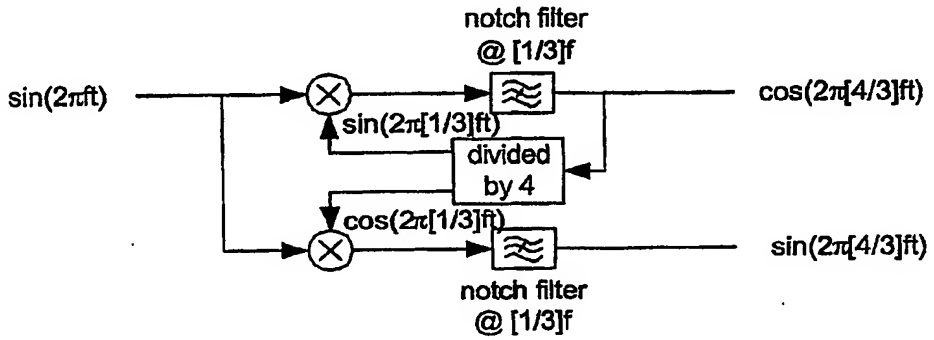


Narrow band



Wide band using wide band poly phase filter

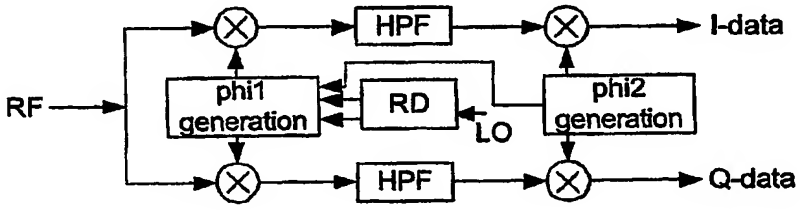
Figure 1: Narrowband and wideband version of a (¾)*LO generator



Narrow band - using notch filter

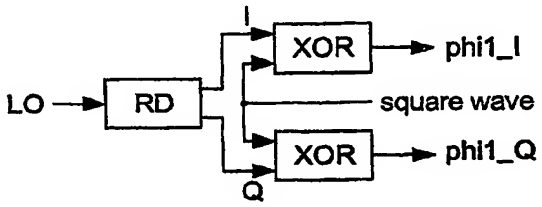
Figure 2: Narrow band using a notch filter

In Sirific's down conversion method – see Fig. 3. In this configuration 3/4LO is used to generate phi_1 – i.e. instead of 2 times the carrier frequency – one method has been proposed in the Fig. 4. This figure uses a square wave to generate phi1 along with XOR gates. The square can be generated from a frequency-controlled oscillator. This square wave may have the ability of changing frequency and its "digital" pattern – however this waveform has to have an average value of zero (assuming it is swinging between +1 and –1).



General implementation of
using RD within Sirific's core

Figure 3: Using a regenerator divider (RD) within Sirific's core



example of generating phi1 using
RD element

Figure 4: A method of generating phi1_I and phi1_Q using a square wave. The square wave can be generated using Sirific's "Sogen" block. Sogen can also generated phi2

ARCHITECTURE DESCRIPTION

The version that will be implemented within Silicon is the wide band version in Figure 1.

The divided by four elements and the mixer configuration will cause the frequency component at f, to be multiplied with a square wave at frequency f/3. The square waves will be denoted as g_c for the cosine branch and g_s for the sine branch. Under ideal conditions and ideal matched conditions, the quadrature summing elements can be represented by the Fig 5.

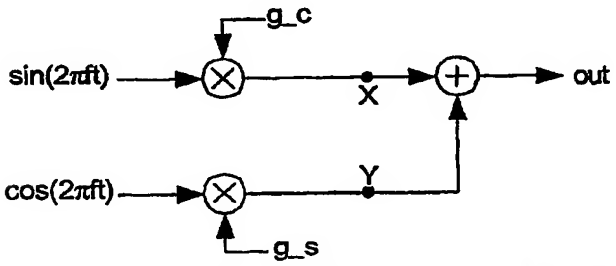


Fig. 5: Summing elements with square wave inputs g_c and g_s.

The output is summarized in the table below:

CA 02415917 2003-01-08

Table I: Output of Fig. 5, where fund is 4/3*f

Nth tone	Relative mag	[illegible]	[illegible]
1	1	(4/3)*f	fund
3	1/3	0*f	DC
5	1/5	(8/3)*f	2*fund
7	1/7	(4/3)*f	fund
9	1/9	4*f	3*fund
11	1/11	(8/3)*f	2*fund
13	1/13	4*f	3*fund
15	1/15	4*f	3*fund

SYSTEM LEVEL DESIGN

The blocks that need implementing are the following:

1. A linear wide band single to differential converter (range of 525-1875MHz)
2. A wide band poly phase filter over a frequency range 525-1875MHz
3. A linear mixer
4. A divided by 4 element
5. XOR block to implement phi1_I and phi1_Q
6. Incorporate the sogen block
7. Buffers to drive the LO ports of the mixers

The top-level block diagram is shown in Fig. 6.

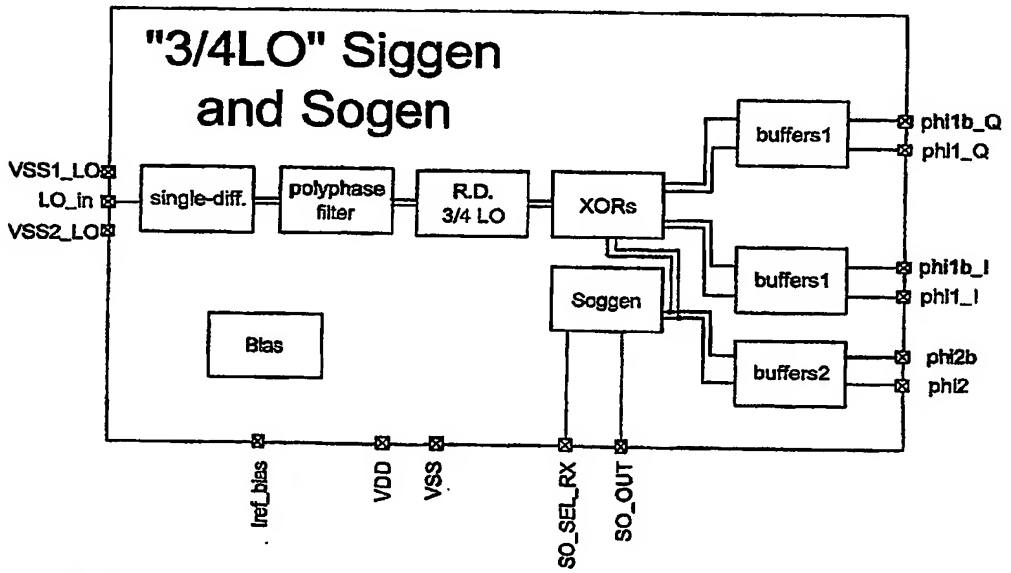


Fig. 6: Top level block diagram of "3/4LO" Siggen and Sogen.

TABLE II: Current estimates and frequency range of components

Element	Estimated current (mA)	Min frequency (MHz)	Max frequency (MHz)	Voltage range (mV)	
				Min	Max
Single-diff.	1	525	1875		
Poly phase	0	525	1875		
RD	2	525	2500		
XORs	1	700	2500		
Soggen	1	25	175		
Buffers1	3	700	2500	1200	1800
Buffers2	3	25	150	0	1800
TOTAL	**14**	**NA**	**NA**		

Appendix A

Local Oscillator Generation Scheme in 0.18 μm CMOS for Low-IF and Direct Conversion Architectures

Local Oscillator Generation Scheme in 0.18 µm CMOS for Low-IF and Direct Conversion Architectures

Sathwant Dosanjh, William Kung[§], Tajinder Manku[§], Christopher Snyder[§]

University of Waterloo, Waterloo, Ontario, N2L 3G1, Canada
[§]SiRiFIC Wireless Corporation, Waterloo, Ontario, N2J 5J2, Canada

Abstract — **A fully-integrated, ratio-based local oscillator (LO) generation scheme using regenerative division is described. Using 0.18 µm CMOS technology, the core LO system consumes 27 mW from a 1.8 V supply. The entire chip is fully integrated, including on-chip spiral inductors; harmonic rejection mixers are also employed to suppress unwanted mixing products to better than -36 dBc. Across an RF band of 150 MHz, a quadrature phase error of less than 2° and a maximum image suppression of 36 dB is achieved. Using a 4/3 multiplication factor to generate the local oscillator, LO-RF interactions are reduced and an LO-RF leakage of -86 dBm has been measured at the mixer input. This system can be utilized in low-IF or direct conversion architectures.**

I. Introduction

The demand to provide low cost wireless solutions has created much interest in direct conversion architectures. Furthermore, with the long term goal of integrating digital processing on-chip, CMOS is the technology of choice.

Designing a fully-integrated direct conversion receiver in CMOS is not without challenges. In a direct conversion receiver, the local oscillator operates at the same frequency as the received carrier. Thus RF-LO leakage can couple to the on-chip voltage controlled oscillator (VCO) and degrade receiver performance, especially in phase-modulated systems. LO-RF leakage through the substrate can cause LO re-radiation and produce undesirable DC offsets. Furthermore, CMOS technology offers passive components with low quality factor and low self-resonant frequencies, which can pose problems for the realization of higher frequency (eg. 5 GHz) designs. As such, careful LO planning is essential to the design of a direct conversion receiver.

This paper describes the design of a fractional-based LO generation scheme in a 1.8 V, 0.18 µm, single-poly, 6-metal bulk CMOS process for direct conversion or low-IF architectures. On-chip spiral inductors and harmonic-rejection mixers are used to suppress unwanted mixing products. The LO system is implemented along with direct down-conversion mixers to facilitate testing.

II. LO Generation

In [1] and [2], an offset LO scheme is described whereby a 2/3 multiplication factor is used for the GSM band and a 4/3 multiplication factor for the DCS/PCS band. For frequency and phase modulated signals, the down-conversion must be done in quadrature to retain all information. Since the LO is not generated in quadrature, a polyphase circuit is inserted in the received RF signal path; this polyphase would add loss and noise to the system [3].

An LO scheme based on regenerative division, also utilizing a 4/3 multiplication factor, is described in [4] and [5]. The architecture of a system based on regenerative division is shown in Fig. 1. This architecture requires a polyphase filter at the output to generate quadrature LO.

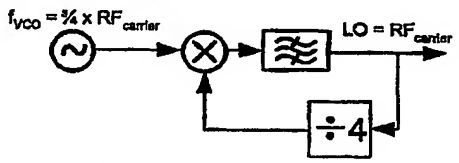


Fig. 1. Regenerative divider for VCO frequency at ¾ $RF_{carrier}$.

The proposed LO generation system, which also uses the technique of regenerative division [6], provides quadrature LO signals (a polyphase filter at the output is not needed) and employs harmonic-rejection mixers (HRM) [7]. This architecture is shown in Fig. 2. All signal paths are fully differential.

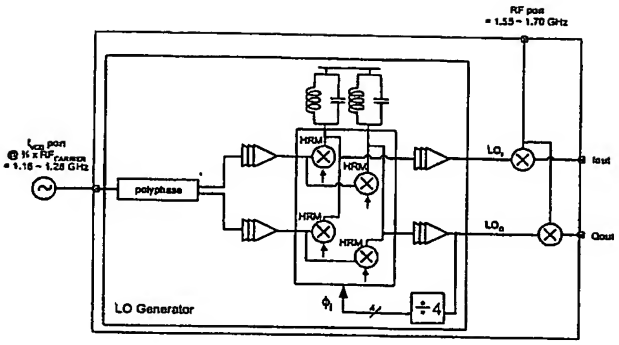


Fig. 2. System diagram of down-converter using LO generation scheme.

III. LO CIRCUITRY

A. Polyphase Filter

The VCO frequency is applied to the f_{VCO} port at 3/4 times the RF carrier frequency. A stagger-tuned four-stage polyphase filter is used to generate quadrature signals from 600 to 1795 MHz. To account for the loss of the polyphase filter, it is followed by a gain stage, which consists of a common-source, differential amplifier. This is shown in Fig. 3.

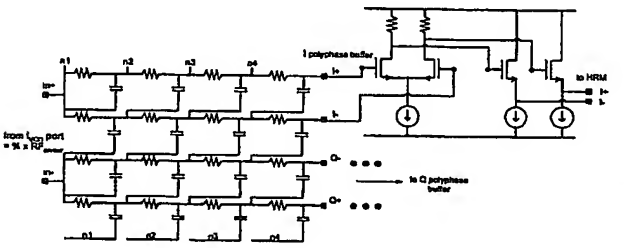


Fig. 3. Circuit diagram of 4-section polyphase filter and gain stage.

B. Harmonic Rejection Mixers

A divide-by-four circuit is used in feedback with a set of mixers to generate the 4/3 multiplication factor. A tuned LC tank forms the load for the HRMs and is used to suppress the unwanted mixing products generated as a result of the harmonics produced by the divide-by-four circuit. An 8.2 nH inductor with a quality factor of 4.5 was designed, using ASITIC [8]. HRMs were employed, to relax the filtering requirements of the LC tank. The HRM reduces the mixer products generated by the 3rd and 5th harmonics of the divide-by-four circuit. The HRMs are based on Gilbert-cell mixers as shown in Fig. 4. The phase delayed signals (Φ_i) required by the HRMs are naturally provided by the divide-by-four circuit. The Φ_i signals are weighted and delayed, as described in [7], to achieve correct harmonic cancellation.

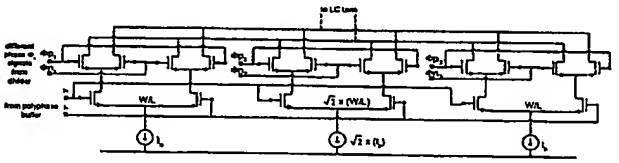


Fig. 4. Circuit diagram of harmonic-rejection mixer.

The inputs to the HRM are applied in quadrature to two sets of HRM pairs. This reduces various mixer products and also provides quadrature LO outputs. The quadrature LO signals are applied to a pair of down-conversion mixers, which provide baseband in-phase and quadrature outputs.

IV. MEASURED RESULTS

A die photo of the implemented system is shown in Fig. 5. The system, excluding the pad frame, occupies an area of approximately 1.5 mm^2.

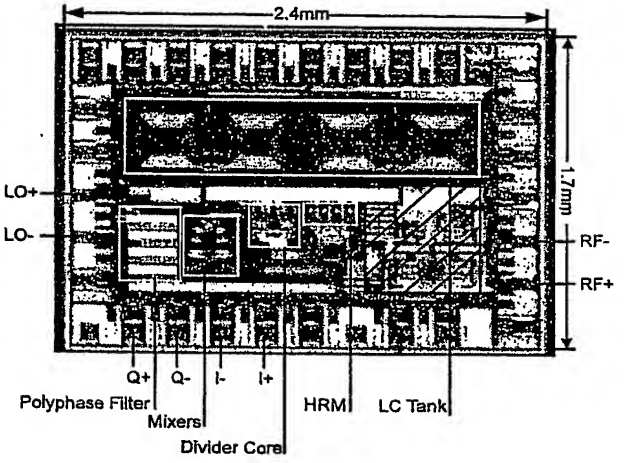


Fig. 5. Die photo of LO generation system and down-conversion mixers.

Across an input f_{VCO} range of 1.16 to 1.28 GHz (equivalent to the down-conversion of an RF band between 1.55 to 1.70 GHz), the measured quadrature error is shown in Fig. 6. All data is plotted versus the frequency that was applied to the f_{VCO} port of the chip.

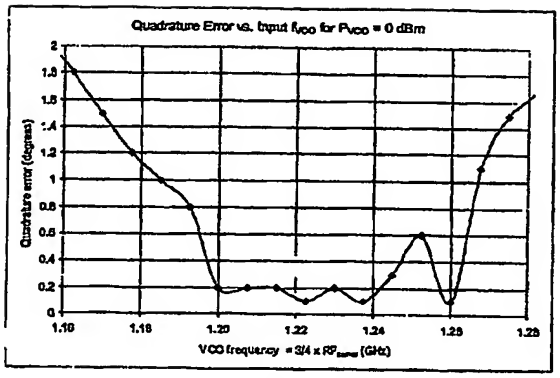


Fig. 6. Quadrature error vs. input LO frequency.

A quadrature error of less than 2° is achieved over the entire frequency range.

This system could also be used in a low-IF architecture. The equivalent unwanted image suppression of this down-conversion system has been calculated based on the measured phase and amplitude mismatch, and is shown in Fig. 7.

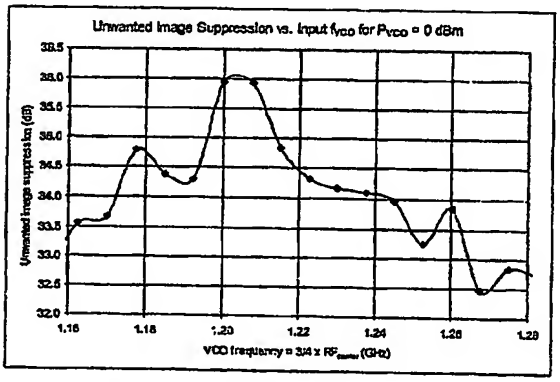


Fig. 7. Calculated unwanted image suppression vs. input LO frequency.

As stated, the HRMs are utilized to reduce the mixer products generated as a result of the 3rd and 5th harmonic outputs from the divide-by-four circuit. These are situated at 3/4 x $RF_{carrier}$ and 5/4 x $RF_{carrier}$, and mix with the input LO, at 3/4 x $RF_{carrier}$ to generate unwanted products at the following fractions of the $RF_{carrier}$: 1/2, 3/2, and 2; these products were measured to be -36 dBc, -51 dBc, and -49 dBc, respectively.

A. Results Summary

TABLE I
SUMMARY OF MEASURED RESULTS

Total power consumption at 1.8 V	45 mW
Core LO circuit power consumption at 1.8 V	27 mW
RF band	1.55 – 1.70 GHz
f_{VCO} range required	1.16 – 1.28 GHz
Quadrature error (P_{VCO} = 0 dBm)	< 2°
Amplitude mismatch (P_{VCO} = 0 dBm)	< 0.37 dB
Equivalent Unwanted Image Suppression	> 32 dB
LO-RF leakage (0 dBm applied at 1.23 GHz)	-86 dBm at 1.64 GHz at mixer inputs
RF-LO leakage (-10 dBm at 1.64 GHz)	-72 dBm
Harmonic rejection at 1/2 x $RF_{carrier}$	-36 dBc
3/2 x $RF_{carrier}$	-51 dBc
2 x $RF_{carrier}$	-49 dBc
Circuit Area (excluding pad frame)	1.6 mm^2
Technology	0.18 µm CMOS

A VCO frequency of 3/4 x $RF_{carrier}$, or 1.16 to 1.28 GHz, is needed, to operate in an RF band from 1.55 to 1.70 GHz and generate the required LO for direct conversion or low-IF architectures. A phase error of less than 2°, with greater than an equivalent 32 dB image suppression is achieved across this band. An LO-RF leakage of -86 dBm was measured at the mixer input ports. This was achieved in a 1.8 V, 0.18 µm, single-poly, 6-metal bulk CMOS process.

V. CONCLUSION

This paper describes the implementation of a ratio-based LO generation scheme in a 1.8 V, 0.18 µm, single-poly, 6-metal bulk CMOS process for direct conversion or low-IF architectures. On-chip spiral inductors and harmonic-rejection mixers are used to improve the spurious response.

ACKNOWLEDGEMENT

The authors wish to acknowledge the assistance of T. Charania, D. Hoang, B. Hogg, K. Konanur, T. Mantell, D. Marchesan, S. Walsh, and G. Weale.

REFERENCES

[1] A. Molnar et. al, "A Single Chip Quad Band (850/900/1800/1900MHz) Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N

Synthesizer," ISSCC 2002, International Solid-State Circuits Conference, pp. 184 – 185, February 2002, San Francisco.

[2] R. Magoon and A Molnar, "RF Local Oscillator Path for GSM Direct Conversion Transceiver with True 50% Duty Cycle Divide by Three and Active Third Harmonic Cancellation," RFIC Symposium Digest of Papers. pp. 23 - 26, 2002.

[3] F. Behbahani et al., "CMOS Mixers and Polyphase Filters for Large Image Rejection," IEEE J. Solid-State Circuits, vol. 36, pp. 873 – 886, June, 2001.

[4] D. Grant, "Solving the Direct Conversion Problem," Planet Analog, Aug., 2001.

[5] J. Strange and S. Atkinson, "A Direct Conversion Transceiver for Multi-Band GSM Application," RFIC Symposium Digest of Papers. pp. 25 - 28, 2000.

[6] R. Miller, "Fractional-Frequency Generators Utilizing Regenerative Modulation," Proc. I.R.E, vol. 27, pp. 446 – 457, July, 1939.

[7] J. A. Weldon et. al., "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter with Harmonic-Rejection Mixers," IEEE J. Solid-State Circuits, vol. 36, pp. 2003-2015, Dec., 2001.

[8] A. Niknejad and R. Meyer, "Analysis, Design, and Optimization of Spiral Inductors and Transformers for RF IC's," IEEE J. Solid-State Circuits, vol. 33, pp. 1470 – 1481, Oct., 1998.